Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1-20 (canceled)

21. (new) An arrangement for converting a binary input signal corresponding to an n-bit thermometer code into a binary output code, the arrangement comprising:

a first number of OR gate circuits configured to receive bits of the n-bit thermometer code;

a first adder operably coupled to receive output signals from the first number of OR gates, the first adder operable to provide at an output at least one binary output signal of the binary output code;

a second number of multiplexer circuits having data inputs configured to receive bits of the thermometer code, the second number of multiplexer circuits further including at least one selection input operably coupled to receive at least one binary output signal from the first adder;

a second adder operably connected downstream of the multiplexer circuits to receive a multiplexer output therefrom, the second adder operable to provide at an output thereof at least one further binary output signal of the output binary code.

22. (new) The arrangement according to claim 21, wherein the first number of OR gate circuits is defined by a number of inputs of each of the first number of OR gates and the number of bits *n* in the n-bit thermometer code.

23. (new) The arrangement according to claim 21, wherein the n-bit thermometer code is divided into a plurality of m segments, each segment having an identical bit width k.

24. (new) The arrangement according to claim 23, wherein each of the first number of OR gate circuits is configured to receive only bits of a single segment of the n-bit thermometer code.

25. (new) The arrangement according to claim 24, wherein each of the second number of multiplexer circuits are configured to receive only a single bit from any one segment of the n-bit thermometer code.

26. (new) The arrangement according to claim 23, wherein the first number of OR gate circuits comprises m-1 OR gate circuits.

27. (new) The arrangement according to claim 23, wherein the second number of multiplexer circuits comprises k-1 multiplexer circuits.

28. (new) The arrangement according to claim 23, wherein the first adder is has m-1 inputs and the second adder includes m-1 inputs.

29. (new) The arrangement according to claim 21,

wherein at least one of the first adder and the second adder comprises a full adder.

30. (new) The arrangement according to claim 21, wherein each of the adders, the OR gate circuits, and the multiplexer circuits have a circuit construction defined from a standard cell from a digital circuit library.

31. (new) The arrangement according to claim 23, wherein the converter has m output terminals.

32. (new) The arrangement according to claim 21, wherein the binary output code comprises at least one of a binary code and a hexadecimal code.

33. (new) A method for converting a binary input signal corresponding to a thermometer code into a binary output code, the method comprising:

(a) receiving an n-bit thermometer code;

(b) dividing the n-bit thermometer code into m segments;

(c) performing an OR operation on bits of at least the m-1 more significant segments to generate at least m-1 output signals;

(d) summing the at least m-1 output signals, a binary result from this addition forming a first part of the binary output code;

(e) multiplexing sets of bits of different segments, each set comprising bits having the same MSB significance within their respective segments, wherein the first part of the output code is used as multiplex selection signal;

(f) adding the multiplexed output signals, a binary result from this addition forming a second part of the binary output code.

34. The method according to claim 33, wherein step (c) further comprises performing the OR operation on the bits of only the m-1 more significant segments.

35. The method according to claim 34, wherein the sets of bits of step (e) exclude a least significant bit of each segment.

36. The method according to claim 33, wherein the sets of bits of step (e) exclude a least significant bit of each segment.

37. Method according to claim 33 wherein step (b) further comprises dividing the n-bit thermometer code into m segments, each segment having a bit width k.

38. An analog-to-digital converter, comprising

at least one analog input for coupling at least one analog input signal into an input stage,

a reference stage connected downstream of the input stage, the reference stage configured to generate a n-bit thermometer code representative of the at least one analog input signal, and

at least one converter configured to convert the n-bit thermometer code into a binary output code, each converter comprising,

a first number of OR gate circuits configured to receive bits of the n-bit thermometer code,

a first adder operably coupled to receive output signals from the first number of OR gates, the first adder operable to provide at an output at least one binary output signal of the binary output code,

a second number of multiplexer circuits having data inputs configured to receive bits of the thermometer code, the second number of multiplexer circuits further including at least one selection input operably coupled to receive at least one binary output signal from the first adder, and

a second adder operably connected downstream of the multiplexer circuits to receive a multiplexer output therefrom, the second adder operable to provide at an output thereof at least one further binary output signal of the output binary code.

39. (new) The analog-to-digital converter according to claim 38, wherein:

the n-bit thermometer code comprises m segments, each segment having a bit width k, and

the first number of OR gate circuits comprises m-1 OR gate circuits.

40. (new) The analog-to-digital converter according to claim 39, wherein the second number of multiplexer circuits comprises k-1 multiplexer circuits.

II. Conclusion

Applicant respectfully requests entry of the amendment and favorable consideration of the application.

A prompt and favorable action on the merits is requested.

Respectfully Submitted,

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